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| EXAMINER | |
|---|---|
| TRAN, MICHAEL THANH | |
| ART UNIT | PAPER NUMBER |
| 2827 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/599,514 | PENG ET AL. | |
| | Examiner | Art Unit | |
| | MICHAEL T. TRAN | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. In response to the Communications dated December 10, 2007, claims 1-22, 24 and 25 are active in this application.

### *Specification*

2. If there are cross-reference to related applications, please include the respective patent numbers, if known.

### *Claim Rejections- 35 U.S.C. § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claim 1 is rejected under 35 U.S.C 102(e) as being anticipated by Nakamura et al. [U.S. Patent # 6,956,766].

With respect to claim 1, Nakamura et al. disclose, in the figures, a control method of an MRAM (Magnetoresistive Random Access Memory) based on vertical current

writing [current I of figure 2], wherein the writing operation of information in a magnetic film cell MFC of the MRAM is implemented by corporate effect of a current parallel [see figure 1] to the MFC and vertical to an easy magnetization direction of the MFC [see figure 2] and a part of said current being branched vertical to the MFC and passing through the MFC [see "Background of the Invention" and "Detailed Description", especially the 4th paragraph].

5. Claims 2-8 and 25 are rejected under 35 U.S.C 102(e) as being anticipated by Nakamura et al. [U.S. Patent # 6,956,766].

With respect to claim 2, Nakamura et al. disclose, in the figures, an MRAM based on vertical current writing, comprising: a) a memory control unit array [figure 30] composed of transistor ATR (4) units [200 of figure 30], the control unit array being integrated in a semiconductor substrate [inherent]; b) a memory cell array [10 of figure 30] composed of a magnetic film ceil MFC (2) [figure 2]; c) contact holes (3e, 3f) and a transitional metal layer [110 of figure 28], the magnetic film cell MFC (2) being connected to the transistor ATR (4) units through the transitional metal layer and the contact holes (3e, 3f) and d) a word line WL (3d) [WLn+1 of figure 30] and a bit line BL (3a) [BLs of figure 30], characterized in that the bit line BL (3a) being arranged above on the magnetic film cell MFC (2) [see figure 28 – bitlines and wordlines are 120], directly connected with the magnetic film cell MFC (2), and vertical to an easy magnetization direction of the magnetic film cell MFC (2)r wherein the writing operation of the information of the maqnetic film cell MFC (2) is implemented by corporate

effect of a current parallel to the MFC(2) in the bit line BL (3a) and a current branched from the bit line BL (3a) vertical to the MFC and passing through the MFC [see "Background of the Invention" and "Detailed Description", especially the 4th paragraph].

With respect to claim 3, Nakamura et al. disclose, in the figures, one or more current-limiting mechanisms are connected to each bit line BL and are arranged in a peripheral circuit of the MRAM array. It is noted that there exists circuitries coupled to bitlines and wordlines. These circuitries are interpreted as being able to limiting the current by controlling the selected cells/arrays.

With respect to claim 4, Nakamura et al. disclose, in the figures, structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers [C1 and A of figure 2] and a nonmagnetic material layer [B1 of figure 2] interposed between the two magnetic material layers, and stored information is represented and stored by the magnetization state of one of the magnetic material layers.

With respect to claim 5, Nakamura et al. disclose, in the figures, the bit line BL (3a) and the word line WL (3d) are vertical to each other. See figure 30.

With respect to claim 6, Nakamura et al. disclose, in the figures, the word line WL (3d) also acts as the gate of the transistor ATR (4) unit. See figure 30.

With respect to claim 7, Nakamura et al. disclose, in the figures, in the process of reading information, the transistor ATR (4) is turned on and a read current is introduced from the bit line BL (3a) so as to obtain the information stored in the magnetic film cell MFC (2). See Detailed Description regarding reading.

With respect to claim 8, Nakamura et al. disclose, in the figures, there are altogether two internal metal wiring layers [BL/WL of figure 30], i.e., a layer (Sd) where the bit line BL (3a) locates and a layer (5b) where the transitional metal layer (3b} [120 of figure 28] and the ground line GND (3c) [110 of figure 28] locate.

With respect to claim 25, Nakamura et al. disclose, in the figures, said current-limiting mechanism can be constituted by a diode and/or a transistor. Figure 30 shows a transistor being coupled to the array for controlling the respective read/write operations.

6. Claims 9-15 are rejected under 35 U.S.C 102(e) as being anticipated by Nakamura et al. [U.S. Patent # 6,956,766].

With respect to claim 9, Nakamura et al. disclose, in the figures, an MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, comprising: a) a memory read/write control unit array [10 of figure 30] composed of transistor ATR (4) units [TR of figure 30], the read/write control unit being integrated in a semiconductor substrate [see figure 28]; b) a memory cell array composed of a magnetic film cell MFC (2) [see figure 2]; c) contact holes (3e, 3f) [inherent]; and d) a word line WL (3d) and two bit lines BLI (3a) and BL2 (3g) [BLs/WLs of figure 30], wherein a transitional metal layer (3b) [110 of figure 28], the magnetic film cell MFC (2) is connected to the transistor ATR (4) unit through the transitional metal layer (3b) and the contact hole (3f); the bit lines BL! {3a) and BL2 (3g) are isolated by insulation

medium and are parallel to each other in direction [B1 of figure 2], and meantime the bit line BL2 (3g) is connected directly to the magnetic film cell MFC (2) [see figure 2].

With respect to claim 10, Nakamura et al. disclose, in the figures, the basic structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers [C1 and A of figure 2] and a nonmagnetic material layer [B1 of figure 2] interposed between the two magnetic material layers, and the stored information is represented and stored by the magnetization state of one of the magnetic material layers.

With respect to claim 11, Nakamura et al. disclose, in the figures, the directions of the bit lines BLI (3a) and BL2 (3g) are vertical to an easy magnetization direction of the magnetic film cell MFC (2), and are vertical to the direction of the word line WL (3d). See Detailed Description and figures 2, 28 and 30.

With respect to claim 12, Nakamura et al. disclose, in the figures, the word line WL (3d) also acts as the gate of the transistor ATR (4) unit. See figure 30.

With respect to claim 13, Nakamura et al. disclose, in the figures, in the process of reading information, the transistor ATR (4) unit is turned on and a read current is introduced from the bit line BL2 (3g) so as to obtain the information stored in the magnetic film cell MFC (2). See Detailed Description regarding reading operation.

With respect to claim 14, Nakamura et al. disclose, in the figures, the process of its writing operation is implemented by corporate effect of a current parallel to the magnetic film cell MFC (2) on the bit line BLI (3a) and a current introduced from the bit line BL2 (3g), vertical to the magnetic film cell MFC (2) and passing through the

magnetic film cell MFC (2). See Detailed Description regarding programming and figures 2, 28 and 30.

With respect to claim 15, Nakamura et al. disclose, in the figures, there are altogether three internal metal wiring layers, i.e., a layer where the bit line BL (3a) locates, a layer where the bit line BL (3g) locates and a layer where the transitional metal layer (3b) and the ground line GND (3c) locate. See figure 28 - bitlines and wordlines in 120 and ground lower layer 110.

7. Claims 16-22 and 24 are rejected under 35 U.S.C 102(e) as being anticipated by Nakamura et al. [U.S. Patent # 6,956,766].

With respect to claim 16, Nakamura et al. disclose, in the figures, an MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, comprising: a) a memory read/write control unit array composed of transistor ATR (4) units [see figure 30], the read/write control unit array being integrated in a semiconductor substrate [see figure 28]; b) a memory cell array composed of a magnetic film cell MFC (2) [see figure 2]; c) contact holes (3e, 3f) [inherent]; and d) two word lines WLl (3d) and WL2 (3g) and a bit line BL (3a), wherein the word line WL2 (3g) being connected directly to the magnetic film cell MFC (2) and vertical to the bit line BL (3a) [see figure 30], and the bit line BL (3a) being vertical to an easy magnetization direction of the maqnetic film cell MFC {2) [see figure 2], wherein the writing operation of the information of the magnetic film cell MFC (2) is implemented by corporate effect of a current parallel to the maqnetic film cell MFC (2) on the bit line BL (3a) and a current

introduced from the word line WL2 (3g), vertical to the magnetic film cell MFC (2) and passing throuqh the magnetic film cell MFC (2). See Detailed Description regarding programming and figures 2, 28 and 30.

With respect to claim 17, Nakamura et al. disclose, in the figures, the basic structure of the magnetic film cell MFC {2) is constituted by two magnetic material layers [C1 and A of figure 2] and a nonmagnetic material layer [B1 of figure 2] interposed between the two magnetic material layers, and the stored information is represented and stored by the magnetization state of one of the magnetic material layers. See Detailed Description regarding reading and figures 2, 28 and 30.

With respect to claim 18, Nakamura et al. disclose, in the figures, the bit line BL (3a) [BL of figure 30] is vertical to the word lines WLI (3d) and WL2 (3g) in parallel [WLs of figure 30]. See figure 30.

With respect to claim 19, Nakamura et al. disclose, in the figures, the bit line BL (3a) is arranged above on the word line WL2 (3g) and is isolated from it by insulation. See figures 28 and 30.

With respect to claim 20, Nakamura et al. disclose, in the figures, the word line WL (3d} also acts as the gate of the transistor ATR (4) unit. See figure 30.

With respect to claim 21, Nakamura et al. disclose, in the figures, in the process of reading informationr the transistor ATR (4) is turned on and a read current is introduced from the word line WL2 (3g) so as to obtain the information stored in the magnetic film cell MFC (2) . See Detailed Description regarding reading and figures 2, 28 and 30.

With respect to claim 22, Nakamura et al. disclose, in the figures, comprising a transitional metal layer (3b), the magnetic film cell MFC (2) being connected to the transistor ATR (4) unit through the
transitional metal layer (3b) and the contact hole (3f). See figures 2, 28 and 30.

With respect to claim 24, Nakamura et al. disclose, in the figures, there are altogether three internal metal wiring layers, i.e., a layer where the bit line BL (3a) locates, a layer where the word line WL2 (3g) locates and a layer where the transitional metal layer (3b) and the ground line GND (3c) locate. See figure 28 - bitlines and wordlines in 120 and ground lower layer 110.

***Conclusion***

8. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. .Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. .Any inquiry of a general nature or relating to the status of this application. should be directed to the Group receptionist whose telephone number is (571) 272-1650.

/Michael T. Tran/
Michael T. Tran
Art Unit 2827
March 6, 2008